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PATENT
ATTORNEY DOCKET NO.: 053785-5053-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
	)	
Gee Sung CHAE et al.	)	Confirmation No. 3202
	)	
Application No.: 10/730,133	)	Art Unit: 2871
	)	
Filed: December 9, 2003	)	Examiner: M. Ton
	)	
For: ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY SUBSTRATE HAVING HIGH APERTURE RATIO AND METHOD FOR FABRICATING THE SAME	)	**Mail Stop Appeal Brief - Patents**

Commissioner for Patents
U.S. Patent and Trademark Office
Mail Stop Appeal Brief-Patents
Alexandria, VA 22314

REVISED APPELLANTS' BRIEF TRANSMITTAL FORM

1. Transmitted herewith is the Appellants' *Revised* Brief Under 37 C.F.R. § 41.31, which is being submitted in response to the Notification of Non-Compliant Appeal Brief dated August 9, 2006.

2. Additional papers enclosed.

   - ☐ Drawings: ☐ Formal ☐ Informal (Corrections)
   - ☐ Information Disclosure Statement
   - ☐ Form PTO-1449, ___ references included
   - ☐ Citations
   - ☐ Declaration of Biological Deposit
   - ☐ Submission of "Sequence Listing", computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.

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3. Oral Hearing Under 37 C.F.R. 1.194

   - ☐ Oral hearing is hereby requested.
   - ☐ Fee under 37 C.F.R. 1.17(d) is enclosed.

4. Extension of time

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ Appellants petition for an extension of time, the fees for which are set out in 37 CFR 1.17(a)-(d), for the total number of months checked below:

Total months requested	Fee for extension	[fee for Small Entity]
☐ one month	$ 120.00	$ 60.00
☐ two months	$ 450.00	$ 225.00
☐ three months	$ 1,020.00	$ 510.00
☐ four months	$1,590.00	$ 795.00
☐ five months	$2,160.00	$1,080.00

Extension of time fee due with this request: **$120.00**

If an additional extension of time is required, please consider this a Petition therefor.

5. Fee Payment

☒ No fee is to be paid at this time.

☐ The Commissioner is hereby authorized to charge $($ for the -month extension of time fee and $ for the Appellants' Brief filing fee due) to Deposit Account No. 50-0310.

☒ The Commissioner is hereby authorized to charge any fees including fees due under 37 CFR 1.16 and 1.17 which may be required, or credit any overpayment to Deposit Account No. 50-0310.

Respectfully submitted,

MORGAN, LEWIS & BOCKIUS LLP

Date: August 17, 2006

By: _____
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REVISED APPELLANTS' BRIEF UNDER 37 C.F.R. § 41.31

This *revised* Brief is in response to the Notification of Non-Compliant Appeal Brief mailed August 9, 2006, in the above-identified patent application. Although no fee set forth under 37 C.F.R. § 41.20(b)(2) is being filed concurrently herewith, Appellants hereby authorize the Commissioner to charge any additional fees which may be required, including fees due under 37 C.F.R. §§ 1.16 and 1.17, to Deposit Account 50-0310.

1. The Real Party In Interest

The real party in interest in this appeal is LG.Philips LCD Co, Ltd. of Seoul, Korea.

2. Related Appeals and Interferences

Appellants respectfully advise that an Appeal Brief has been filed in the corresponding parent application (10/133,320). Appellants respectfully assert that this appealed parent application may directly affect, or be directly affected by, or have a bearing on the Board's decision in the appeal of the present application.

3. Status of Claims

The status of the claims is as follows:

Claims rejected: 13-21 and 34-58.
Claims objected to: none.
Claims allowed: none.
Claims withdrawn: none.
Claims canceled: 1-12 and 22-33.
Claims appealed: 13-21 and 34-58.

4. Status of Amendments

All Amendments have been entered to date. Most recently, on February 15, 2006, Appellants filed a Request for Reconsideration under 37 C.F.R. § 1.116 in response to the Final Office Action dated November 15, 2005. Subsequently, the Examiner issued an Advisory Action which indicated that the Request for Reconsideration under 37 C.F.R. § 1.116 was considered but did not place the application in condition for allowance. Appellants filed a Notice of Appeal on May 8, 2006. Accordingly, appealed claims are attached as Claims Appendix to this *revised* brief.

5. Summary of the Claimed Subject Matter

An aspect of Appellants' present invention relates generally to an array substrate for a liquid crystal display device and a method for fabricating an array substrate for a liquid crystal display device.

Independent Claim 13

With respect to independent claim 13, as discussed in Appellants' specification from paragraph [0034] on page 14 to paragraph [0041] on page 18 and shown in FIGs. 5-8, and with respect to FIGs. 5 and 6, as well as FIGs. 7 and 8 (as provided in parenthesis), a liquid crystal display device includes a first transparent substrate 110 (210), a second transparent substrate 190 (290) facing the first transparent substrate 110 (210), a gate line 121 (221) arranged on the first transparent substrate 110 (210) along a first direction, the gate line 121 (221) includes a gate electrode 122 (222) extending from the gate line 121 (221) by a predetermined length along a second direction perpendicular to the first direction, a data line 161 (261) arranged on the first transparent substrate 110 (210) along a second direction perpendicular to the first direction, the gate line 121 (221) and the data line 161 (261) perpendicularly crossing each other and defining a pixel region P2 (P3), a thin film transistor arranged on the first transparent substrate 110 (210) and adjacent to the pixel region P2 (P3), the thin film transistor electrically connected to both the gate line 121 (221) and the data line 161 (261), a common line 125 (225) arranged on the first transparent substrate 110 (210) along the first direction parallel with and adjacent to the gate line 121 (221), the common line 125 (225) having a protrusion extending toward the gate line 121 (221) along the second direction spaced apart from the gate line 121 (221) by a predetermined distance, a first

capacitor electrode 165 (265) overlapping a portion of the common line 125 (225) and the protrusion of the common line 125 (225) to form a first storage capacitor 171 (271), the first capacitor electrode 165 (265) connected to the thin film transistor, a pixel electrode 181 (281) formed within the pixel region P2 (P3), the pixel electrode 181 (281) contacting the first capacitor electrode 171 (271), a black matrix 191 (291) on the second transparent substrate 190 (290), the black matrix 191 (291) covering the thin film transistor, the protrusion of the common line 125 (225), and portions of the gate line 121 (221) and common line 125 (225), and a common electrode 192 (292) on the second transparent substrate 190 (290) to cover the black matrix 191 (291), wherein the predetermined length of the gate electrode 122 (222) is greater than the predetermined distance between the protrusion and the gate line 121 (221).

Independent Claim 34

With regard to independent claim 34, as discussed in Appellants' specification from paragraph [0034] on page 14 to paragraph [0041] on page 18 and shown in FIGs. 5-8, and with respect to FIGs. 5 and 6, as well as FIGs. 7 and 8 (as provided in parenthesis), a method for fabricating a liquid crystal display device includes steps of forming a gate line 121 (221) on a first transparent substrate 110 (210) along a first direction, the gate line 121 (221) includes a gate electrode 122 (222) extending from the gate line 121 (221) by a predetermined length along a second direction perpendicular to the first direction, forming a data line 161 (261) on the first transparent substrate 110 (210) along a second direction perpendicular to the first direction, the gate line 121 (221) and the data line 161 (261) perpendicularly crossing each other and defining a pixel region P2 (P3), forming a thin film transistor on the first transparent substrate 110 (210) and adjacent to the pixel region P2 (P3),

the thin film transistor is electrically connected to both the gate line 121 (221) and the data line 161 (261), forming a common line 125 (225) on the first transparent substrate 110 (210) along the first direction parallel with and adjacent to the gate line 121 (221), the common line 125 (225) having a protrusion extending toward the gate line 121 (221) along the second direction spaced apart from the gate line 121 (221) by a predetermined distance, forming a first capacitor electrode 165 (265) to overlap a portion of the common line 125 (225) and the protrusion of the common line 125 (225) to form a first storage capacitor 171 (271), the first capacitor electrode 165 (265) connected to the thin film transistor, forming a pixel electrode 181 (281) within the pixel region P2 (P3), the pixel electrode 181 (281) contacting the first capacitor electrode 165 (265), forming a black matrix 191 (291) on a second transparent substrate 190 (290), the black matrix 191 (291) covering the thin film transistor, the protrusion of the common line 125 (225), and portions of the gate line 121 (221) and common line 125 (225), forming a common electrode 192 (292) on the second transparent substrate 190 (290) to cover the black matrix 191 (291), and forming the first substrate 110 (210) to face the second substrate 190 (290), wherein the predetermined length of the gate electrode 122 (222) is greater than the predetermined distance between the protrusion and the gate line 121 (221).

Independent Claim 43

With regard to independent claim 43, as discussed in Appellants' specification from paragraph [0034] on page 14 to paragraph [0041] on page 18 and shown in FIGs. 5-8, and with respect to FIGs. 5 and 6, as well as FIGs. 7 and 8 (as provided in parenthesis), a liquid crystal display device includes a first transparent substrate 110 (210), a second transparent

substrate 190 (290) facing the first transparent substrate 110 (210), a gate line 121 (221) arranged on the first transparent substrate 110 (210) along a first direction, a data line 161 (261) arranged on the first transparent substrate 110 (210) along a second direction perpendicular to the first direction, the gate line 121 (221) and the data line 161 (261) perpendicularly crossing each other and defining a pixel region P2 (P3), a thin film transistor arranged on the first transparent substrate 110 (210) and adjacent to the pixel region P2 (P3), the thin film transistor electrically connected to both the gate line 121 (221) and the data line 161 (261), a common line 125 (225) arranged on the first transparent substrate 110 (210) along the first direction parallel with and adjacent to the gate line 121 (221), a protrusion extending from the common line 125 (225) toward the gate line 121 (221) along the second direction, a pixel electrode 181 (281) formed within the pixel region P2 (P3), a black matrix 191 (291) on the second transparent substrate 190 (290), the black matrix 191 (291) covering the thin film transistor and portions of the gate line 121 (221) and common line 125 (225), and a common electrode 192 (292) on the second transparent substrate 190 (290) to cover the black matrix 191 (291), wherein the black matrix 191 (291) covers an area between the gate line 121 (221) and the protrusion.

Independent Claim 51

With regard to independent claim 51, as discussed in Appellants' specification from paragraph [0034] on page 14 to paragraph [0041] on page 18 and shown in FIGs. 5-8, and with respect to FIGs. 5 and 6, as well as FIGs. 7 and 8 (as provided in parenthesis), a method of fabricating a liquid crystal display device includes a first transparent substrate 110 (210), a second transparent substrate 190 (290) facing the first transparent substrate 110 (210),

forming a gate line 121 (221) arranged on a first transparent substrate 110 (210) along a first direction, forming a data line 161 (261) arranged on the first transparent substrate 110 (210) along a second direction perpendicular to the first direction, the gate line 121 (221) and the data line 161 (261) perpendicularly crossing each other and defining a pixel region P2 (P3), forming a thin film transistor on the first transparent substrate 110 (210) and adjacent to the pixel region P2 (P3), the thin film transistor electrically connected to both the gate line 121 (221) and the data line 161 (261), forming a common line 125 (225) on the first transparent substrate 110 (210) along the first direction parallel with and adjacent to the gate line 121 (221), the common line 125 (225) includes a protrusion extending from the common line 125 (225) toward the gate line along the second direction, forming a pixel electrode 181 (281) formed within the pixel region P2 (P3), forming a black matrix 191 (291) on a second transparent substrate 190 (290), the black matrix 191 (291) covering the thin film transistor and portions of the gate line 121 (221) and common line 125 (225), and forming a common electrode 192 (292) on the second transparent substrate 190 (290) to cover the black matrix 191 (291), wherein the black matrix 191 (291) covers an area between the gate line 121 (221) and the protrusion.

6. Grounds of Rejection To Be Reviewed On Appeal

Claims 13-16, 20, 21, 34-44, and 48-58 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujikawa et al. (US 5,995,177) in view of Hebiguchi (US 6,091,473), Kaneko et al. (US 6,587,162), and Fujiwara et al. (US 5,835,170).

Appellants respectfully note that the Final Office Action dated November 15, 2005 (at page 3) actually excludes identification of claims 38, 39, and 40 in the heading of the above-rejection, although the body of the above-rejection (at page 7) makes mention of "[a]s to claims 34-42 and 51-58." Accordingly, Appellants have now revised the exact heading of the rejection to correct this deficiency.

Claims 17-19 and 45-47 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujikawa et al. in view of Hebiguchi, Kaneko et al., and Kawamoto et al. (US 5,151,806).

7. Argument

(i) Rejections under 35 U.S.C. § 112, first paragraph

No claims are presently rejected under 35 U.S.C. § 112, first paragraph.

(ii) Rejections under 35 U.S.C. § 112, second paragraph

No claims are presently rejected under 35 U.S.C. § 112, second paragraph.

(iii) Rejections under 35 U.S.C. § 102

No claims are presently rejected under 35 U.S.C. § 102.

(iv) Rejections under 35 U.S.C. § 103

Claims 13-16, 20, 21, 34-37, 41-44, and 48-58 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujikawa et al. (US 5,995,177) in view of Hebiguchi (US 6,091,473), Kaneko et al. (US 6,587,162), and Fujiwara et al. (US 5,835,170). Appellants respectfully traverse this rejection for the following reasons.

The Final Office Action acknowledges the numerous deficiencies of Fujikawa et al. including:

> Fujikawa does not appear to explicitly specify that the storage capacitance common line has a protrusion and a first capacitor electrode overlaps a portion of the common line and protrusion of the common line to form a first storage capacitor, the first capacitor electrode connected to the thin film transistor.

Final Office Action at page 4.

> Fujikawa does not appear to explicitly specify a black matrix on the second transparent substrate, the black matrix covering the thin film transistor, the protrusion of the common line, and portions of the gate line and the common line and a common electrode on the second transparent substrate to cover the black matrix.

Final Office Action at page 5.

> Fujikawa does not appear to explicitly specify that *the gate line includes a gate electrode extending from the gate line by a predetermined length along a second direction perpendicular to the first direction* and the common line protrusion *extending toward the gate line along the second direction spaced apart from the gate line by a predetermined distance* and *wherein the predetermined length of the gate electrode is greater than the predetermined distance between the protrusion and the gate line*.

Final Office Action at page 6 (Emphasis in original).

Accordingly, the Final Office Action relies upon each of Hebiguchi, Kaneko et al., and Fujiwara to remedy the individual deficiencies of Fujikawa, as detailed and acknowledged above. Thus, the Final Office Action concludes that it would have been obvious to one of ordinary skill in the art of liquid crystals to modify Fujikawa for various reasons to arrive at Applicants' claimed invention. Appellants respectfully traverse these rejections for at least the following reasons.

With regard to Hebiguchi, the Final Office Action relies upon Hebiguchi to allegedly teach common electrodes extending from a common electrode wiring line and a capacity structure "so that capacity is secured and capacity generated by the capacity generating electrodes functions as the removal of the effect of parasitic capacity when liquid crystal is driven and storage capacity for holding signal voltage (Column 6, Lines 30-49)." In addition, the Final Office Action alleges that "Hebiguchi is evidence that ordinary workers in the field of liquid crystals would have had the reason, suggestion, and motivation to overlap a capacity generating electrode with a common electrode protruding from a common electrode wiring line and connecting the capacity generating electrode and drain for securing capacity and for removal of the effect of parasitic capacity when liquid crystal is driven and storage capacity for holding signal voltage." Thus, the Final Office Action concludes that "it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Fujikawa in view of Hebiguchi for an array substrate in which capacity is secured, the effects of parasitic capacity are removed, and for storage capacity for holding signal voltage." Appellants respectfully traverse this portion of the rejection for at least the following reasons.

First, Appellants respectfully assert that Fujikawa et al. is directed toward an active matrix substrate of an LCD device having pixel and common electrodes disposed on opposing substrates, i.e., a twisted neumatic (TN) LCD device; whereas Hebiguchi et al. is directed toward an active matrix substrate of an LCD device having pixel and common electrodes disposed on a single substrate, i.e., an in-plane switching (IPS) LCD device. Accordingly, Appellants respectfully assert that Fujikawa et al. and Hebiguchi et al. are directed to completely non-analogous technologies, and as such, one of ordinary skill in the

art would not look to structures of an IPS LCD device to modify the structure of a TN LCD device. Thus, Appellants respectfully assert that the Final Office Action has not established any proper motivation to modify the TN LCD device of Fujikawa et al. with the IPS LCD device of Hebiguchi et al., and thus, has further not established a *prima facie* case of obviousness.

Second, Appellants respectfully assert that modifying the TN LCD device of Fujikawa et al. with the teachings of an IPS LCD device of Hebiguchi et al. would render the TN LCD device of Fujikawa et al. unsatisfactory for its intended purpose. Specifically, Appellants respectfully assert that following the teachings of Hebiguchi et al., with regard to relative disposition of the common line and alleged protrusions extending from the common line of the IPS LCD device, would cause significant detrimental capacitive influences upon the pixel electrode of the TN LCD device of Fujikawa et al., i.e., parasitic capacitance coupling. Accordingly, modifying the TN LCD device of Fujikawa et al. to form a common line and protrusions extending from the common line would induce detrimental capacitive influences upon the pixel electrode of Fujikawa et al., which would render the TN LCD device of Fujikawa et al. inoperable and unsatisfactory for its intended purpose. Thus, Appellants respectfully assert that the Final Office Action has not established any proper motivation to modify the TN LCD device of Fujikawa et al., and thus, has further not established a *prima facie* case of obviousness.

Third, Appellants respectfully assert that Hebiguchi et al. fails to provide any proper motivation with which to modify Fujikawa et al. For example, the Final Office Action alleges that "Hebiguchi has this structure so that capacity is secured and capacity generated by the capacity generating electrodes functions as the removal of the effect of parasitic

capacity when liquid crystal is driven and storage capacity for holding signal voltage (Column 6, Lines 30-49)." However, Appellants respectfully assert that the IPS LCD structures disclosed by Hebiguchi et al. are wholly incompatible with the TN LCD structure disclosed by Fujikawa et al. Specifically, incorporating the capacity generating electrode 65 of Hebiguchi et al. would cause undesirable parasitic capacitive coupling with the pixel electrode of Fujikawa et al., thereby resulting in an inoperable TN LCD device. Accordingly, because modifying the TN LCD device of Fujikawa et al. to form a capacity generating electrode would induce detrimental capacitive influences upon the pixel electrode of Fujikawa et al., which would render the TN LCD device of Fujikawa et al. inoperable and unsatisfactory for its intended purpose, Appellants respectfully assert that the Final Office Action has not established any proper motivation to modify the TN LCD device of Fujikawa et al., and thus, has further not established a *prima facie* case of obviousness.

Thus, for at least the above reasons Appellants respectfully assert that the Final Office Action has failed to establish a *prima facie* case of obviousness with regard to Appellants' claimed invention.

With regard to Kaneko et al., the Final Office Action relies upon Kaneko et al. for allegedly teaching and disclosing "a liquid crystal display wherein a black matrix is formed on an opposing substrate and shields portions of a gate line and drain line and furthermore shields a common line (Column 3, Lines 60-65 and Column 4, Lines 9-12)." In addition, the Final Office Action relies upon Kaneko et al. for allegedly teaching "that typically a black matrix is formed on an upper color filter substrate and has a common electrode layer over a black matrix (Column 1, Lines 46-49)." Accordingly, the Final Office Action concludes that these alleged teachings and disclosures by Kaneko et al. of "a configuration of the black

matrix with respect to the gate line and common line contributes to improved yield by preventing disconnection from occurring in a layered line portion of lead terminal portion of an active matrix liquid crystal display device (Column 1, Lines 5-12)." Furthermore, the Final Office Action alleges that "Kaneko is evidence that ordinary workers in the field of liquid crystals would have found the reason, suggestion and motivation to specify a black matrix on the second transparent substrate, the black matrix covering the thin film transistor, the protrusion of the common line, and portions of the gate line and the common line and a common electrode on the second transparent substrate to cover the black matrix for improving yield by preventing disconnection from occurring in a layered line portion or lead terminal portion of an active matrix liquid crystal display device (Column 1, Lines 5-12)." Thus, the Final Office Action concludes that "[it] would have been obvious to one or ordinary skill in the art of liquid crystals at the time the invention was made to modify Fujikawa in view of Kaneko for improved yield by preventing disconnection from occurring in a layered line portion or lead terminal portion of an active matrix liquid crystal display device (Column 1, Lines 5-12)." Appellants respectfully traverse this portion of the rejection for at least the following reasons.

First, Appellants respectfully assert that the allegation that Kaneko et al. teaches and discloses both a black matrix that shields portions of gate and drain lines and, simultaneously, a common line at "Column 3, Lines 60-65 and Column 4, Lines 9-12" is completely taken out of context with regard to the complete disclosure of Kaneko et al. Specifically, Kaneko et al. discloses, under the heading "Summary of the Invention," an apparent second embodiment, wherein:

> (2) A liquid crystal display comprising, a pair of substrates, a liquid crystal layer interposed between said pair of substrates, a gate line formed on one of said pair of substrate, a first insulating layer formed over said gate line, a drain line formed on said first insulating layer, a second insulating layer formed over said drain line, a pair of electrodes disposed between said liquid crystal layer and one of said pair of substrates, **wherein a black matrix formed on another of said pair of substrates and shielding said gate line and said drain line**, and a portion of said drain line is intersected with said gate line, and an electrically conductive layer is formed on said second insulating layer and covering at least said portion (emphasis added).

In addition, Kaneko et al. discloses, under the heading "Summary of the Invention," an apparent third embodiment, wherein:

> (3) A liquid crystal display comprising, a pair of substrates, a liquid crystal layer interposed between said pair of substrates, a gate line formed on one of said pair of substrate, a common line formed on one of said pair of substrate, a first insulating layer formed on said common line, a drain line formed on said first insulating layer, a second insulating layer formed on said drain line, a pixel electrode formed on said first insulating layer, a counter electrode formed on one of said pair of substrates, wherein a portion of said drain line is intersected with said common line, and **a black matrix formed on another of said pair of substrates and shielding said common line and said drain line**, and an electrically conductive layer is formed on said second insulating layer and covered at least said portion (emphasis added).

Accordingly, Appellants respectfully assert that the above disclosures of Kaneko et al. are separate and mutually distinct from each other. Thus, Appellants respectfully assert that Kaneko et al. fails to teach or suggest any single embodiment including "a liquid crystal display wherein a black matrix is formed on an opposing substrate and shields portions of a gate line and drain line and furthermore shields a common line," as alleged by the Final Office Action. Moreover, Appellants respectfully assert that Kaneko et al. is completely silent with regard to any disclosure of an *aggregate teaching* of mixing various features of the different disclosed embodiments of Kaneko et al. Therefore, Appellants respectfully

assert that the Final Office Action fails to establish a *prima facie* case of obviousness with regard to Appellants' claimed invention.

Second, the Final Office Action's allegation that Kaneko et al. allegedly teaches "[s]uch a configuration of the black matrix with respect to the gate line and common line contributes to improved yield by preventing disconnection from occurring in a layered line portion of lead terminal portion of an active matrix liquid crystal display device (Column 1, Lines 5-12)" is completely taken out of context with regard to the full disclosure of Kaneko et al. Specifically, Kaneko et al. discloses, under the heading "Background of the Invention" and under the sub-heading "Field of the Invention" at col. 1, lines 5-12, that:

> The present invention relates to a liquid crystal display device and, more particularly, to a liquid crystal display device which is improved in yield factor by preventing disconnection from occurring in a layered line portion or a lead terminal portion in a liquid crystal display device of an active matrix type such as a thin-film transistor (TFT) type.

In addition, Kaneko et al. explicitly discloses, at col. 6, lines 26-31, that:

> According to each of the constructions of the invention, it is possible to efficiently prevent disconnection or the like due to electrolytic corrosion or stress caused by the penetration of moisture toward the gate line, the drain line, the intersection of both lines in the pixel area or the conductor layer of a lead terminal.

Furthermore, Kaneko et al. explicitly discloses, at col. 6, lines 53-60, that:

> In the invention, at the same time that pixel electrodes are formed, a capping layer (protective layer: also called a cap layer) made of a transparent conductive layer is formed over the portion of a passivation layer in which electrolytic corrosion easily occurs. If a pinhole is formed in a portion of the passivation layer, the pinhole is buried by a pattern of the transparent conductive layer formed in that portion, whereby the supply of moisture is intercepted.

Accordingly, Appellants respectfully assert that the complete disclosure of Kaneko et al. reveals that it is the capping layer (i.e., protective layer) that provides the benefits of "a liquid crystal display device which is improved in yield factor by preventing disconnection from occurring in a layered line portion or a lead terminal portion in a liquid crystal display device of an active matrix type such as a thin-film transistor (TFT) type," and **NOT** the relative disposition of the black matrix with regard to the data, drain, and/or common line or common electrode. Thus, Appellants respectfully assert that the alleged motivation to modify Fujikawa et al., as set forth in the Final Office Action, is completely incorrect and a gross misinterpretation of the disclosure of Kaneko et al. Therefore, Appellants respectfully assert that the Final Office Action further fails to establish a *prima facie* case of obviousness with regard to Appellants' claimed invention.

Third, for at least the reasons set forth above, the Final Office Action alleges that "Kaneko is evidence that ordinary workers in the field of liquid crystals would have found the reason, suggestion and motivation to specify a black matrix on the second transparent substrate, the black matrix covering the thin film transistor, the protrusion of the common line, and portions of the gate line and the common line and a common electrode on the second transparent substrate to cover the black matrix for improving yield by preventing disconnection from occurring in a layered line portion or lead terminal portion of an active matrix liquid crystal display device (Column 1, Lines 5-12)" is completely unsupported by the full disclosure of Kaneko et al. Accordingly, since the Final Office Action's alleged motivation is false and a complete distortion of the actual disclosure of Kaneko et al., then the conclusion presented by the Final Office Action that "[it] would have been obvious to one or ordinary skill in the art of liquid crystals at the time the invention was made to modify

Fujikawa in view of Kaneko for improved yield by preventing disconnection from occurring in a layered line portion or lead terminal portion of an active matrix liquid crystal display device (Column 1, Lines 5-12)" is also false. Thus, Appellants respectfully assert that the Final Office Action further fails to establish a *prima facie* case of obviousness with regard to Appellants' claimed invention.

With regard to Fujiwara, the Final Office Action relies upon Fujiwara to allegedly teach "a data line (101) with a protrusion and a gate line (Gn+1) with a protrusion." In addition, the Final Office Action alleges that "[t]he length of the extension from the gate line is longer than the distance between the data line protrusion and gate line." Thus, the Final Office Action concludes that "[i]t would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Fujikawa in view of Fujiwara for a high aperture ratio due to a reduction in size of the storage capacitor thus improving display brightness (Column 5, Lines 55-67)." Appellants respectfully traverse this portion of the rejection for at least the following reasons.

First, Appellants respectfully assert that the Final Office Action's alleged motivation for modifying Fujikawa et al. with the disclosure of Fujiwara is completely unsupported by the disclosure of Fujiwara. Appellants respectfully assert that the allegation that Fujiwara somehow teaches or suggests forming a data line with a protrusion and a gate line with a protrusion for "a high aperture ratio due to a reduction in size of the storage capacitor thus improving display brightness (Column 5, Lines 55-67)" is completely taken out of context with regard to the full disclosure of Fujiwara. Specifically, Fujiwara discloses, at col. 5, lines 55-67, that:

> Furthermore, the storage capacitor employs a gate insulation film of the pixel transistor as an insulation layer. As a result, the gate insulation film has a smaller thickness as compared to a conventional structure employing an interlayer insulation film in the lower layer of the pixel electrode. Consequently, an area required for the storage capacitor C.sub.S can be made smaller than that required for the conventional storage capacitor C.sub.S. Accordingly, **an aperture ratio of the pixel can be made larger due to a reduction in size of the storage capacitor C.sub.S, thereby improving brightness of the liquid crystal display device** (emphasis added).

Accordingly, Appellants respectfully assert that Fujiwara actually discloses that the aperture ratio of the pixel can be increased due to the storage capacitor Cs having a reduced size. Thus, Appellants respectfully assert that Fujiwara fails to disclose *ANYTHING* with regard to forming a data line with a protrusion and a gate line with a protrusion for "a high aperture ratio due to a reduction in size of the storage capacitor thus improving display brightness (Column 5, Lines 55-67)," as alleged by the Final Office Action. Therefore, Appellants respectfully assert that the Final Office Action further fails to establish a *prima facie* case of obviousness with regard to Appellants' claimed invention.

For at least the above reasons, since the Final Office Action fails to meet the requirements for establishing a *prima facie* case of obviousness as to independent claims 13, 34, 43, and 51, claims 13, 34, 43, and 15 are not obvious.

With regard to the Final Office Action's allegation that "it may be presumed that the storage capacitance common line and gate line are of the same material (claim 14) for manufacturing convenience and may include an opaque material as a light shield (claim 15) as consistent with the goal of improving yield as taught by Kaneko et al.," Appellants respectfully traverse the rejection for at least the following reasons.

First, Appellants respectfully assert that the "presumption" made by the Final Office Action is incorrect. Specifically, Appellants respectfully assert that none of the prior art of record, especially Kaneko et al., for at least the reasons detailed above, teach or suggest anything with regard to "manufacturing convenience." Appellants respectfully request that the Examiner clarify the exact logical reasoning, along with fully supporting evidence, to show that the storage capacitance common line and gate line of whichever applied reference may be presumed to be "of the same material...for manufacturing convenience."

Second, if the Examiner is attempting to allege that "manufacturing convenience" is either *well known* or *common knowledge*, then Appellants respectfully disagree. Appellants respectfully assert that, as instructed in MPEP 2144.03A, "[i]t would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known," and, in part, "[i]t is never appropriate to rely solely on 'common knowledge' in the art without evidentiary support in the record, as the principle evidence upon which a rejection was based. *Zurko*, 258 F.3d at 1385, 59 USPQ2d at 1697." Accordingly, Appellants respectfully submit that since none of the prior art of record teaches or suggests that storage capacitance common lines and gate lines made of the same material is well known and capable of instant and unquestionable demonstration as being well-known *for manufacturing convenience*, then it is not appropriate for the Examiner to take official notice or make the assertion that forming storage capacitance common lines and gate lines of the same material is well known.

Furthermore, as instructed by MPEP 2144.03C, "[i]f applicant adequately traverses the examiner's assertion of official notice, the examiner must provide documentary evidence in the next Office Action if the rejection is maintained. See 37 CFR 1.104(c)(2). See also *Zurko*, 258 F.3d at 1386, 59 USPQ2d at 1697." Thus, Appellants respectfully submit that if prosecution of the instant application is reopened and the rejection is maintained, documentary evidence be provided in the next Office Action that it is well-known for forming storage capacitance common lines and gate lines of the same material.

Third, Appellants respectfully assert that the alleged "goal of improving yield as taught by Kaneko" is completely unsupported by Kaneko et al. Specifically, Appellants respectfully assert that Kaneko et al. is completely silent with regard to forming "the storage capacitance common line and gate line are of the same material...for manufacturing convenience and may include an opaque material as a light shield...as consistent with the goal of improving yield as taught by Kaneko." Appellants respectfully request that the Examiner clarify the exact logical reasoning, along with fully supporting evidence, to show that Kaneko et al. explicitly teaches that "the storage capacitance common line and gate line are of the same material...for manufacturing convenience and may include an opaque material as a light shield...as consistent with the goal of improving yield."

For at least the above reasons, since the Final Office Action fails to meet the requirements for establishing a *prima facie* case of obviousness as to claims 14 and 15, claims 14 and 15 are not obvious.

With regard to the Final Office Action's allegation that "it may be presumed that data lines and storage capacitor electrode are formed of the same material simultaneously for manufacturing convenience as taught by Kaneko," Appellants respectfully traverse the rejection for at least the following reasons.

First, Appellants respectfully assert that the "presumption" made by the Final Office Action is incorrect. Specifically, Appellants respectfully assert that none of the prior art of record, especially Kaneko et al., for at least the reasons detailed above, teach or suggest anything with regard to "manufacturing convenience." Appellants respectfully request that the Examiner clarify the exact logical reasoning, along with fully supporting evidence, to show that the data lines and storage capacitor electrode of whichever applied reference may be presumed to be "of the same material...for manufacturing convenience."

Second, if the Examiner is attempting to allege that "manufacturing convenience" is either *well known* or *common knowledge*, than Appellants respectfully disagree. Appellants respectfully assert that, as instructed in MPEP 2144.03A, "[i]t would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known," and, in part, "[i]t is never appropriate to rely solely on 'common knowledge' in the art without evidentiary support in the record, as the principle evidence upon which a rejection was based. *Zurko*, 258 F.3d at 1385, 59 USPQ2d at 1697." Accordingly, Appellants respectfully submit that since none of the prior art of record teaches or suggests that data lines and storage capacitor electrodes are simultaneously made of the same material are well known and capable of instant and unquestionable demonstration as being well-known *for manufacturing convenience*, then it is not appropriate for the Examiner

to take official notice or make the assertion that forming data lines and storage capacitor electrodes simultaneously of the same material is well known.

Furthermore, as instructed by MPEP 2144.03C, "[i]f applicant adequately traverses the examiner's assertion of official notice, the examiner must provide documentary evidence in the next Office Action if the rejection is maintained. See 37 CFR 1.104(c)(2). See also *Zurko*, 258 F.3d at 1386, 59 USPQ2d at 1697." Thus, Appellants respectfully submit that if prosecution of the present application is reopened and the rejection is maintained, documentary evidence be provided in the next Office Action that it is well-known for forming data lines and storage capacitor electrodes simultaneously of the same material.

Thus, Appellants respectfully assert that the alleged motivation "as taught by Kaneko" is completely unsupported by Kaneko et al. Specifically, Appellants respectfully assert that Kaneko et al. is completely silent with regard to "data lines and storage capacitor electrode formed of the same material simultaneously for manufacturing convenience." Appellants respectfully request that the Examiner clarify the exact logical reasoning, along with fully supporting evidence, to show that Kaneko et al. explicitly teaches that "data lines and storage capacitor electrode formed of the same material simultaneously for manufacturing convenience."

For at least the above reasons, since the Final Office Action fails to meet the requirements for establishing a *prima facie* case of obviousness as to claim 16, claim 16 is not obvious.

In rejecting claims 20, 21, and 50, the Final Office Action merely instructs Appellants to "please refer to Figure 1A." Appellants can only surmise that the Examiner is referring to Hebiguchi for allegedly "teaching" the features recited by claims 20, 21, and 50. Appellants

respectfully traverse this portion of the rejection on grounds that the Final Office Action has not established any proper motivation to modify the TN LCD device of Fujikawa et al. with the IPS LCD device of Hebiguchi et al., and thus, has further not established a *prima facie* case of obviousness.

With regard to the Final Office Action's allegation that "Applicant's recited steps of a method for fabricating a liquid crystal display device would have been rendered obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made in light of the device as disclosed and taught in and by the above cited references," Appellants respectfully traverse this portion of the rejection for at least the following reasons.

First, Appellants traverse each and every ground of rejection made in the Final Office Action with regard to the combination of features recited by claims 34-42 and 51-58. Specifically, Appellants respectfully traverse the apparent rejection of claims 34-42 and 51-58 for at least for the grounds presented above with regard to each of Fujikawa et al., Hebiguchi, Kaneko et al., and Fujiwara et al. Thus, Appellants respectfully assert that the Final Office Action further fails to establish a *prima facie* case of obviousness with regard to claims 34-42 and 51-58.

Claims 17-19 and 45-47 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujikawa et al. in view of Hebiguchi, Kaneko et al., and Kawamoto et al. (US 5,151,806). Appellants respectfully traverse these rejections for the following reasons.

With regard to the alleged combined teachings of Fujikawa et al., Hebiguchi, and Kaneko et al., Appellants respectfully assert that the Final Office Action has failed to establish a *prima facie* case of obviousness with regard to at least independent claims 13, 34, 43, and 51. Moreover, Appellants respectfully assert that Kawamoto et al. fails to remedy the

deficiencies of any of Fujikawa et al., Hebiguchi, and Kaneko et al. Thus, Appellants respectfully assert that the Final Office Action fails to establish a *prima facie* case of obviousness with regard to any of claims 17-19 and 45-47.

The Final Office Action acknowledges that "Fujikawa does not appear to explicitly specify... first and second capacitor electrodes simultaneously formed of the same material..." Accordingly, the Final Office Action relies upon Kawamoto et al. for allegedly disclosing "a liquid crystal display apparatus having...to prevent short-circuiting (ABS, entire patent)." In addition, the Final Office Action alleges that "Kawamoto is evidence that ordinary workers in the field of liquid crystals would have had the reason, suggestion, and motivation to include a second capacitor electrode overlapping a portion of a gate line and connected to the pixel electrode to prevent short-circuiting and for storage capacitance." Thus, the Final Office Action concludes that "it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to include the structure of Kawamoto into the array substrate of Fujikawa to prevent short-circuiting and for storage capacitance." Appellants respectfully traverse the rejection for at least the following reasons.

First, Appellants respectfully assert that the Final Office Action has failed to provide any motivation with which to form the first and second capacitor electrodes "simultaneously of the same material," as required by claims 18 and 46. Accordingly, Appellants respectfully assert that the Final Office Action fails to establish a *prima facie* case of obviousness with regard to at least claims 18 and 46.

Second, Appellants respectfully assert that the Final Office Action has failed to identify any prior art reference of record that properly teaches forming first and second capacitor electrodes "simultaneously of the same material," as required by claims 18 and 46.

Accordingly, Appellants respectfully further assert that the Final Office Action fails to establish a *prima facie* case of obviousness with regard to at least claims 18 and 46.

For at least the above reasons, since the Final Office Action fails to meet the requirements for establishing a *prima facie* case of obviousness as to claims 18 and 46, claims 18 and 46 are not obvious.

Since the Final Office Action fails to meet the requirements for establishing a *prima facie* case of obviousness as to independent claims 13, 34, 43, and 51, claims 13, 34, 43, and 51 are not obvious. Furthermore, since claims 14-21, 35-42, 44-50, and 52-58 depend from claims 13, 34, 43, and 51, respectively, and incorporate all the features of claims 13, 34, 43, and 51, claims 14-21, 35-42, 44-50, and 52-58 are not obvious at least for the above reasons for which independent claims 13, 34, 43, and 51 are not obvious. Thus, Appellants respectfully request that the rejections of claims 13-21 and 34-58 under 35 U.S.C. § 103(a) be withdrawn.

(v) Other Rejections

No claims are presently rejected under grounds other than those referred to above.

In view of the foregoing, Appellants respectfully request the reversal of the Examiner's rejection and allowance of the pending claims. If there are any other fees due in connection with the filing of this Appeal Brief, please charge the fees to our Deposit Account No. 50-0310.

If a fee is required for an extension of time under 37 C.F.R. §1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account No. 50-0310.

Respectfully submitted,

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By: _____

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8. Claims Appendix

Claim 13 (Previously Presented): A liquid crystal display device, comprising:

a first transparent substrate;

a second transparent substrate facing the first transparent substrate;

a gate line arranged on the first transparent substrate along a first direction, the gate line includes a gate electrode extending from the gate line by a predetermined length along a second direction perpendicular to the first direction;

a data line arranged on the first transparent substrate along a second direction perpendicular to the first direction, the gate line and the data line perpendicularly crossing each other and defining a pixel region;

a thin film transistor arranged on the first transparent substrate and adjacent to the pixel region, the thin film transistor electrically connected to both the gate line and the data line;

a common line arranged on the first transparent substrate along the first direction parallel with and adjacent to the gate line, the common line having a protrusion extending toward the gate line along the second direction spaced apart from the gate line by a predetermined distance;

a first capacitor electrode overlapping a portion of the common line and the protrusion of the common line to form a first storage capacitor, the first capacitor electrode connected to the thin film transistor;

a pixel electrode formed within the pixel region, the pixel electrode contacting the first capacitor electrode;

a black matrix on the second transparent substrate, the black matrix covering the thin film transistor, the protrusion of the common line, and portions of the gate line and common line; and

a common electrode on the second transparent substrate to cover the black matrix,

wherein the predetermined length of the gate electrode is greater than the predetermined distance between the protrusion and the gate line.

Claim 14 (Original): The device according to claim 13, wherein the common line includes a same material as the gate line.

Claim 15 (Original): The device according to claim 14, wherein the common line and the gate line are simultaneously formed of an opaque metallic material.

Claim 16 (Original): The device according to claim 13, wherein the data line and the first capacitor electrode are simultaneously formed of a same material.

Claim 17 (Original): The device according to claim 13, further comprising a second capacitor electrode overlapping a portion of the gate line to form a second storage capacitor.

Claim 18 (Original): The device according to claim 17, wherein the first capacitor electrode and the second capacitor electrode are simultaneously formed of a same material.

Claim 19 (Original): The device according to claim 17, wherein the second capacitor electrode is electrically connected to the pixel electrode.

Claim 20 (Original): The device according to claim 13, wherein the protrusion extends from the common line toward the gate line along the second direction.

Claim 21 (Original): The device according to claim 20, wherein the protrusion is arranged between the gate line and the common line.

Claim 34 (Previously Presented): A method for fabricating a liquid crystal display device, comprising the steps of:

forming a gate line on a first transparent substrate along a first direction, the gate line includes a gate electrode extending from the gate line by a predetermined length along a second direction perpendicular to the first direction;

forming a data line on the first transparent substrate along a second direction perpendicular to the first direction, the gate line and the data line perpendicularly crossing each other and defining a pixel region;

forming a thin film transistor on the first transparent substrate and adjacent to the pixel region, the thin film transistor is electrically connected to both the gate line and the data line;

forming a common line on the first transparent substrate along the first direction parallel with and adjacent to the gate line, the common line having a protrusion extending toward the gate line along the second direction spaced apart from the gate line by a predetermined distance;

forming a first capacitor electrode to overlap a portion of the common line and the protrusion of the common line to form a first storage capacitor, the first capacitor electrode connected to the thin film transistor;

forming a pixel electrode within the pixel region, the pixel electrode contacting the first capacitor electrode;

forming a black matrix on a second transparent substrate, the black matrix covering the thin film transistor, the protrusion of the common line, and portions of the gate line and common line;

forming a common electrode on the second transparent substrate to cover the black matrix; and

forming the first substrate to face the second substrate,

wherein the predetermined length of the gate electrode is greater than the predetermined distance between the protrusion and the gate line.

Claim 35 (Original): The method according to claim 34, wherein the common line includes a same material as the gate line.

Claim 36 (Original): The method according to claim 35, wherein the common line and the gate line are simultaneously formed of an opaque metallic material.

Claim 37 (Original): The method according to claim 34, wherein the steps of forming the data line and the first capacitor electrode are simultaneously formed of a same material.

Claim 38 (Original): The method according to claim 34, further comprising a step of forming a second capacitor electrode to overlap a portion of the gate line to form a second storage capacitor.

Claim 39 (Original): The method according to claim 38, wherein the step of forming a first capacitor electrode and the step of forming a second capacitor electrode are simultaneously performed using a same material.

Claim 40 (Original): The method according to claim 38, wherein the second capacitor electrode is electrically connected to the pixel electrode.

Claim 41 (Original): The method according to claim 34, wherein the protrusion extends from the common line toward the gate line along the second direction.

Claim 42 (Original): The method according to claim 41, wherein the protrusion is arranged between the gate line and the common line.

Claim 43 (Previously Presented): A liquid crystal display device, comprising:

a first transparent substrate;

a second transparent substrate facing the first transparent substrate;

a gate line arranged on the first transparent substrate along a first direction;

a data line arranged on the first transparent substrate along a second direction perpendicular to the first direction, the gate line and the data line perpendicularly crossing each other and defining a pixel region;

a thin film transistor arranged on the first transparent substrate and adjacent to the pixel region, the thin film transistor electrically connected to both the gate line and the data line;

a common line arranged on the first transparent substrate along the first direction parallel with and adjacent to the gate line;

a protrusion extending from the common line toward the gate line along the second direction;

a pixel electrode formed within the pixel region;

a black matrix on the second transparent substrate, the black matrix covering the thin film transistor and portions of the gate line and common line; and

a common electrode on the second transparent substrate to cover the black matrix,

wherein the black matrix covers an area between the gate line and the protrusion.

Claim 44 (Previously Presented): The device according to claim 43, further comprising a first capacitor electrode overlapping a portion of the common line to form a first storage capacitor, wherein the first capacitor electrode is connected to the thin film transistor.

Claim 45 (Previously Presented): The device according to claim 44, further comprising a second capacitor electrode overlapping a portion of the gate line to form a second storage capacitor.

Claim 46 (Previously Presented): The device according to claim 45, wherein the first capacitor electrode and the second capacitor electrode are simultaneously formed of a same material.

Claim 47 (Previously Presented): The device according to claim 45, wherein the second capacitor electrode is electrically connected to the pixel electrode at a first region.

Claim 48 (Previously Presented): The device according to claim 47, wherein the black matrix overlaps the first region.

Claim 49 (Previously Presented): The device according to claim 43, wherein the common line and the adjacent gate line are separated by a gap and the black matrix overlaps the gap.

Claim 50 (Previously Presented): The device according to claim 43, wherein the protrusion is arranged between the gate line and the common line.

Claim 51 (Previously Presented): A method of fabricating a liquid crystal display device, comprising:

a first transparent substrate;

a second transparent substrate facing the first transparent substrate;

forming a gate line arranged on a first transparent substrate along a first direction;

forming a data line arranged on the first transparent substrate along a second direction perpendicular to the first direction, the gate line and the data line perpendicularly crossing each other and defining a pixel region;

forming a thin film transistor on the first transparent substrate and adjacent to the pixel region, the thin film transistor electrically connected to both the gate line and the data line;

forming a common line on the first transparent substrate along the first direction parallel with and adjacent to the gate line, the common line includes a protrusion extending from the common line toward the gate line along the second direction;

forming a pixel electrode formed within the pixel region;

forming a black matrix on a second transparent substrate, the black matrix covering the thin film transistor and portions of the gate line and common line; and

forming a common electrode on the second transparent substrate to cover the black matrix,

wherein the black matrix covers an area between the gate line and the protrusion.

Claim 52 (Previously Presented): The method according to claim 51, further comprising forming a first capacitor electrode overlapping a portion of the common line to form a first storage capacitor, wherein the first capacitor electrode is connected to the thin film transistor.

Claim 53 (Previously Presented): The method according to claim 52, further comprising forming a second capacitor electrode overlapping a portion of the gate line to form a second storage capacitor.

Claim 54 (Previously Presented): The method according to claim 53, wherein the first capacitor electrode and the second capacitor electrode are simultaneously formed of a same material.

Claim 55 (Previously Presented): The method according to claim 53, wherein the second capacitor electrode is electrically connected to the pixel electrode at a first region.

Claim 56 (Previously Presented): The method according to claim 55, wherein the black matrix overlaps the first region.

Claim 57 (Previously Presented): The method according to claim 51, wherein the common line and the adjacent gate line are separated by a gap and the black matrix overlaps the gap.

Claim 58 (Previously Presented): The method according to claim 51, wherein the protrusion is arranged between the gate line and the common line.

9. Evidence Appendix

No information is appended under this section.

10. Related Proceedings Appendix

No information is appended under this section.